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Design and Analysis of Sense Amplifier Circuits used in High-Performance and Low-Power SRAMs

APPROVED BY
SUPERVISING COMMITTEE:

Supervisor:

Nur A. Touba

Zhigang Pan

Design and Analysis of Sense Amplifier Circuits used in High-Performance and Low-Power SRAMs

by

Sajith Ahamed Palatham-Veedu, B.Tech

Report

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Master of Science in Engineering

The University of Texas at Austin

August 2011

Acknowledgements

I am thankful to Dr Nur Touba for supervising my report and Dr David Pan for agreeing to be the reader. I am also grateful to my family for their strong support without which I won't have been able to complete this work.

Abstract

Design and Analysis of Sense Amplifier Circuits used in High-Performance and Low-Power SRAMs

Sajith Ahamed Palatham-Veedu, M.S.E.

The University of Texas at Austin, 2011

Supervisor: Nur Touba

Performance and power of sense amplifiers have big implications on the speed of caches used in microprocessors as well as power consumption of IPs in low power system on chips. The speed of voltage sense amplifiers are limited by the differential voltage development time on high capacitance SRAM bit-lines. The dynamic power increases with the differential voltage that needs to be developed on the bit-lines. This report explores multiple sense amplifier techniques - in addition to the conventional voltage sense amplifier, it analyzes current sense amplifier, charge transfer sense amplifier as wells as current latched sense amplifier and compares them in speed, area and power consumption to the voltage sense amplifier. A current sense amplifier operates by sensing the bit cell current directly and shows power and area advantages. A charge transfer sense amplifier makes use of charge redistribution between the high capacitance bit-lines and low capacitance sense amplifier output nodes to provide power benefits. This report also explores the design of a six transistor SRAM bit cell. All circuits are designed and simulated on a 45nm CMOS process.

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Chapter 1. Introduction

Static Random Access Memories (SRAMs) are an important component of microprocessors and system-on-chips. SRAMs are used as large caches in microprocessor cores and serve as storage in various IPs on a system-on-chip like graphics, audio, video and image processors. SRAMs used in high performance microprocesssors and graphics chips have high speed requirements. At the same time, SRAMs used in application processors which go into mobile, handheld and consumer devices have very low power requirements. Since SRAMs serve as large storage on these chips, it's very important to get maximum density out of these. Traditionally a large number of SRAM bit cells, up to 1024 in some cases, are connected to a common bit-line to get the highest density and array efficiency. This results in a large capacitance on the bit-lines which necessitates using differential sense amplifiers for speed reasons. Sense amplifiers detect the data being read by sensing a small differential voltage swing on the bit-lines rather than waiting for a full rail-to-rail swing.

Depending on the performance and power requirements, it's very important for the sense amplifiers to operate fast and do so while burning a minimum amount of power. The large bit-line capacitance is a big performance bottleneck. Conventional Voltage Sense Amplifiers need a minimum amount of differential voltage to be developed on the bit-lines for reliable operation. The amount of time required to develop this differential voltage is linearly proportional to bit-line capacitance. The dynamic power consumed in precharging the bit-lines increases with the differential voltage that needs to be developed. Low power requirements of mobile and embedded chips require sense amplifiers which burn less power than the traditional voltage sense amplifier techniques.

This work explores multiple sense amplifiers – Current Sense Amplifier (CSA), Charge Transfer Sense Amplifier (CTSA), Current Latched Sense Amplifier (CLSA) and compares them in speed, area, and power to the Voltage Sense Amplifier (VSA). A current sense amplifier operates by sensing the bit cell current directly rather than waiting on a differential voltage to develop on the bit-lines. The operation of charge transfer sense amplifier is based on charge sharing from the high capacitance bit-lines to the low capacitance sense amplifier nodes.

This report also presents the design of a six transistor bit cell which is used in all the experiments. All work is done in 45nm CMOS technology with a 1V supply. The sense amplifier designs are evaluated in a 128x128 SRAM array with 128 bit cells on the word-line and 128 bit cells connected to the bit-line.

The content is organized as follows. Chapter 2 explores the design of a six transistor SRAM bit cell. Chapter 3 explains the operation and design of different sense amplifiers. Chapter 4 presents the simulation results and the conclusions are given in Chapter 5.

Chapter 2. SRAM 6T Bit Cell Design

The 6T SRAM bit cell shown in Figure 2.1 is composed of six transistors, two bit-lines (BL and BLB) and one word-line (WL). Both bit-lines carry complementary data. A bit of data is read from or written into a bit cell when WL is enabled. The bit cell has two pass-gate transistors (PG1 and PG2) for accessing the cell, two pull-up transistors (PU1 and PU2) and two pull-down driver transistors (PD1 and PD2).

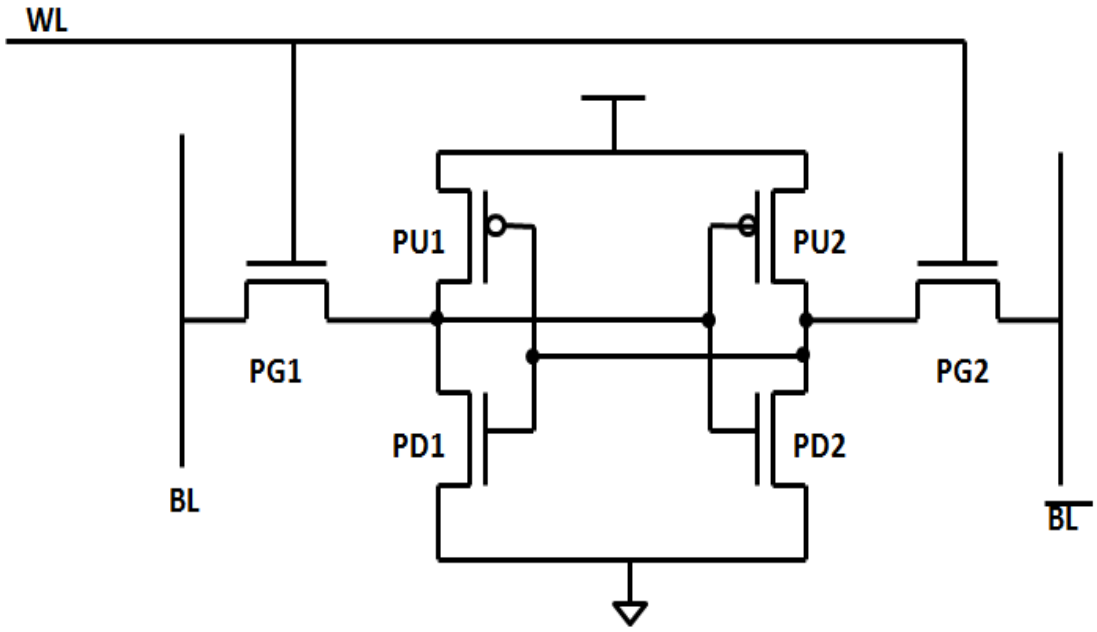


Figure 2.1 6T SRAM Bit Cell

2.1 Read Operation and Read Stability

Before WL is enabled, both bit-lines are precharged high. When WL is enabled, depending on the value stored in the bit cell, one of the two bit-lines is discharged through a PD drive transistor. This creates a differential voltage on the bit-lines, which is captured by a sense amplifier. The bit cell design should ensure sufficient differential is developed on the bit-lines within a specified amount of time.

The read operation exposes storage nodes of the bit cell to the precharged bit-lines. Under this condition, the data stored in the bit cell should not change. This is known as read stability and is an important factor to be considered while designing the bit-cell. During a read operation, the storage node which has a '0' on it rises in voltage due to voltage divider action between the pass-gate PG and pull-down PD transistors. This voltage must remain below the trip point of the cross coupled inverter to ensure internal state is not changed. The level of voltage increase at the internal node is decided by the ratio of the current of the drive transistor PD1 (or PD2) to that of the access transistor PG1 (or PG2). The current ratio between drive transistor and access transistor is called the cell-ratio of the SRAM bit cell. With a large cell-ratio, the voltage on the low state node can be kept low, enhancing read stability of the bit cell. At the same time, increasing cell-ratio also increases the area of the bit cell. Usually, a cell-ratio of 1.5 ~ 2 minimizes bit cell area while ensuring some level of read stability.

2.2 Write Operation and Writability

During a write operation, WL is enabled and the data to be written into the bit cell is driven on the bit lines. The '0'is written first as it is easier for the access transistor PG to fight the weak pull-up PU device than the stronger pull-down PD device which has been sized up for read stability. Once the low going node goes below the trip point of the inverter, the second node goes high completing the write operation.

Writability refers to the requirement that data on bit-lines must change the internal nodes of the bit cell within a specified time. This depends on the ratio of currents of the PU1 (or PU2) and PG1 (or PG2) transistors. To easily switch the internal node voltage to ground, the current of PG1 (or PG2) should be larger than that of PU1 (or PU2). This ratio is called the pull-up ratio, and indicates how easily the data can be changed by the low state bit-line. Pull-up ratio depends on both PMOS and NMOS currents, hence mobility must be considered while sizing the transistors. If NMOS mobility is twice PMOS mobility, same transistor widths can be used for PU1 (or PU2) and PG1 (or PG2) for a pull-up ratio of 0.5.

2.3 Bit Cell Sizing

Based on these design considerations, an SRAM bit cell is designed for 45nm technology as follows. The minimum channel length of the technology is 50nm and the minimum active width is 90nm. The mobility ratio of nmos to pmos is 2:1. For a pull-up ratio of 0.5 and to ensure minimum area, minimum width devices are chosen for PU and PG. A cell-ratio of 1.5 provides a good trade-off between read stability and area. Therefore, the PD device has a width which is 1.5 times that of the PG device. The final sizes are given in the table below.

	Width(nm)	Length(nm)
Pull-Up	90	50
Pull-Down	135	50
PassGate	90	50

Table 2.1 6T Bit Cell Sizing

Chapter 3. Sense Amplifier Techniques

3.1 Voltage Sense Amplifier

A voltage sense amplifier senses the differential voltage on the bit-lines and generates a full rail output. The circuit is shown in Figure 3.1

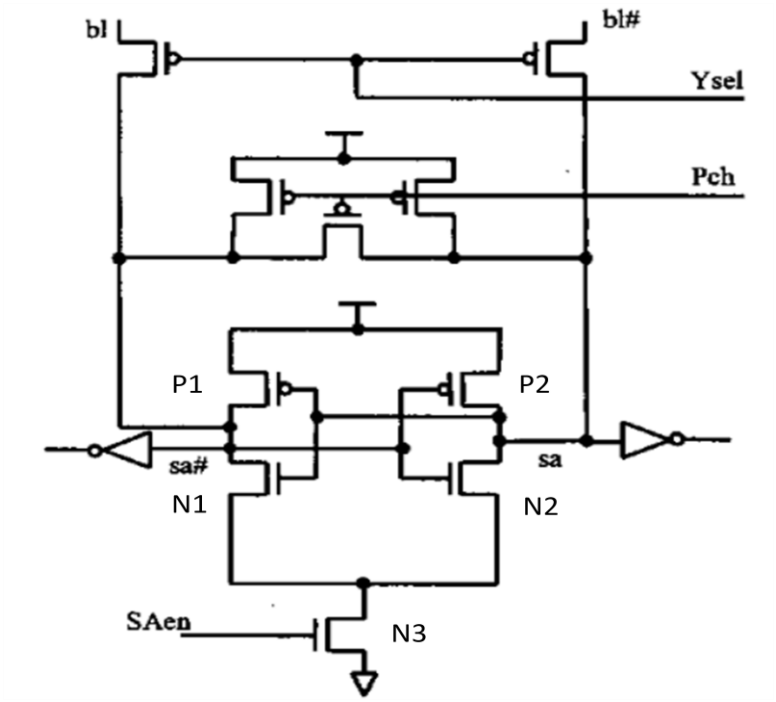


Figure 3.1 Voltage Sense Amplifier [6]

The timing scheme for the voltage sense amplifier is shown in Figure 3.2

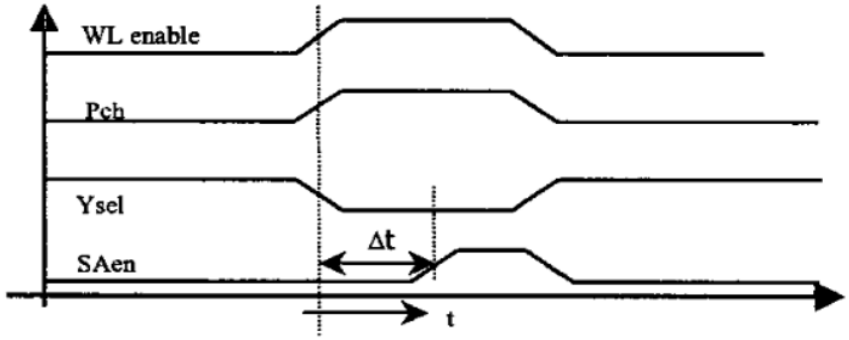


Figure 3.2 Timing Scheme for a Voltage Sense Amplifier [6]

The operation of the circuit is as follows. When WL is enabled, a voltage differential begins to develop on the bl/bl# pair. When enough differential, depending on the technology and circuit, has developed the sense amp enable (SAEN) is activated which causes the cross coupled inverters to go into a positive feedback loop and translate the differential to full rail output. The sense amplifier output node which connects to the bit-line with a lower voltage, for eg sa, is pulled down to 0 while the other output sa# remains high. When sense amplifier is enabled, NMOS devices N1 and N2 go into saturation. The NMOS device N2 which receives full VDD input has a higher current than N1 with a smaller voltage as its Vgs. The one which conducts higher current (N2) pulls its output voltage lower reducing the Vgs on the other NMOS device (N1), which therefore has smaller current flowing through it. This positive feedback loop continues until the output voltage sa has fallen low enough to cause the NMOS device N2 to enter linear region and turn on the PMOS device P1 of the other inverter and cause its output to be driven high. N1 is eventually turned OFF, and the cross coupled inverters store the resulting output.

3.2 Current Sense Amplifier

The current sense amplifier (CSA) operates by sensing the bit cell current directly. It is not dependent on a differential voltage developing across the bit-lines. This helps reduce bit-line precharge power since the low going bit-line can be clamped at a higher voltage than would be required with a voltage sense amplifier. The current sense amplifier consists of two parts: a current transporting circuit with unity gain current transfer characteristics and a sensing circuit which senses the differential current. The circuit diagram of the current sense amplifier is shown in Figure 3.3. It is designed with a combination of ideas from [1] and [5].

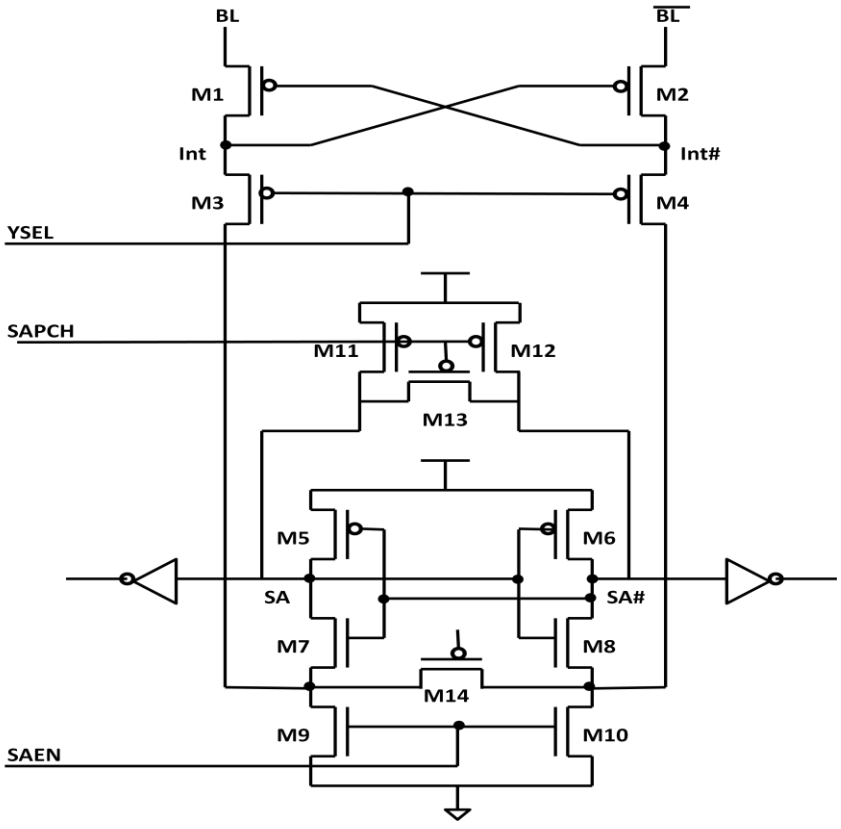


Figure 3.3 Current Sense Amplifier

The current transporting circuit or the current conveyor consists of four equally sized PMOS transistors (P1 through P4) with positive feedback. These devices operate in saturation. The current conveyor circuit, shown in Figure 3.4, operates as follows. The gate-source voltage of M1 will be equal to that of M3, since their currents are equal, their sizes are equal, and both transistors are in saturation. Let this voltage be represented by V1. Similarly, the gate-source voltages of M2 and M4 are also equal, let this be

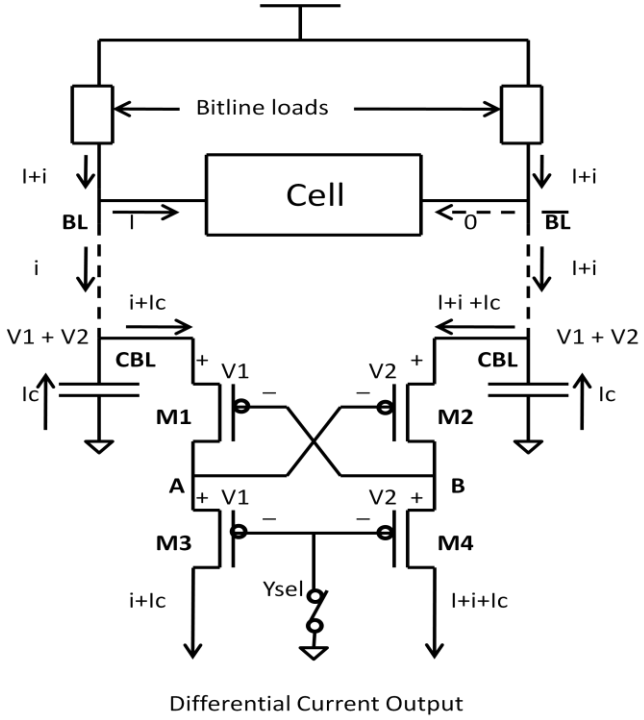


Figure 3.4 Current Conveyor Circuit [2]

represented by V2. When YSEL is grounded, the voltage on BL is given by V1+V2, so is the voltage on BL#. Therefore, the potential of the bit-lines will be equal independent of the current distribution. This means that there exists a virtual short circuit across the bit-lines. Since the bit-line voltages are equal, the bit-line load currents will also be equal, as

well as the bit-line capacitor currents. Since the cell draws a current I, the right leg of the current conveyor draws more current than the left leg. The difference between these two currents will be equal to the cell current. The drain current of M3 and M4 are passed to the current conveyor output which is connected to the current sensing circuit. The differential output current of the current conveyor is therefore equal to the cell current.

The current sense amplifier operates in two phases: precharge and evaluate. During the precharge phase, the bit-lines are precharged through precharge devices connected to the bit-lines (not shown here). The sense amplifier output nodes SA and SA# are also precharged high through M11 and M12 PMOS devices. Devices M11 and M13 are ON during precharge, equalizing the inputs and outputs of the sensing circuit respectively. The operating current of the sense amplifier is determined by the sizes of devices M5-M8. At the end of the precharge phase, precharge and equalization devices M11-M14 are turned OFF. During the evaluation phase, YSEL is pulled low and SAEN is pulled high. The cross coupled inverters comprising of devices M5-M8 then form a high gain positive feedback amplifier. Due to the positive feedback, the impedance looking into the source terminal of either M7 or M8 is a negative resistance, which causes M7 and M8 to begin sourcing a portion of the difference current. The difference current flowing through M7 and M8 flows through the small equivalent capacitance at the drains of M7 and M8, giving rise to a voltage difference across the output nodes of the sense amplifier. The initial trajectory for the magnitude of the voltage difference between the drains of M7 and M8 is given by

$$d\Delta V/dt = 2\Delta I/Cd$$

where Cd is the total capacitance at the drain node of M7 or M8. This trajectory is followed for a short time, and then the resulting differential voltage at the output of the

sense amplifier is rapidly amplified by the positive feedback of the cross coupled inverters, driving one output to zero and keeping the other one high.

The sensing delay is relatively insensitive to bit-line capacitance as the operation is not dependent on the development of a differential voltage across the bit-lines. Unlike the voltage sense amplifier, the output nodes are not tied to the high capacitance bit-lines and are able to respond very quickly. The CSA can have lower voltage swing on bit-lines. This is because the cross coupled PMOS pair M1 and M2 cuts off the discharge path to ground for both bit-lines. Suppose BL is high and BL# is going low. This causes nodes Int and A to go high causing M2 to be cut off. Therefore, the path from the low going BL# to ground is cut off, reducing the voltage swing on it.

3.3 Charge Transfer Sense Amplifier

The Charge Transfer Sense Amplifier (CTSA) operates by making use of the charge redistribution from high capacitance bit-lines to the low capacitance sense amplifier output nodes. This results in high speed operation and lower power consumption due to low voltage swing on the bit-lines. The circuit diagram of a CTSA is shown in Figure 3.5.

3.3.1 Charge Transfer Theory

The basic concept behind charge-transfer amplification is to produce voltage gain by exploiting charge conservation among capacitive devices. For a series connection of two capacitive elements in a system for which charge is conserved, the product of the voltage across the first element and its capacitance must equal the product of the voltage across the second element and its capacitance as shown in the following equation.

$$C_{small} V_{small} = Q = C_{large} V_{large}$$

Voltage gain is therefore realized since a small change in voltage across the larger capacitive element will produce a larger change in voltage across the smaller capacitive element.

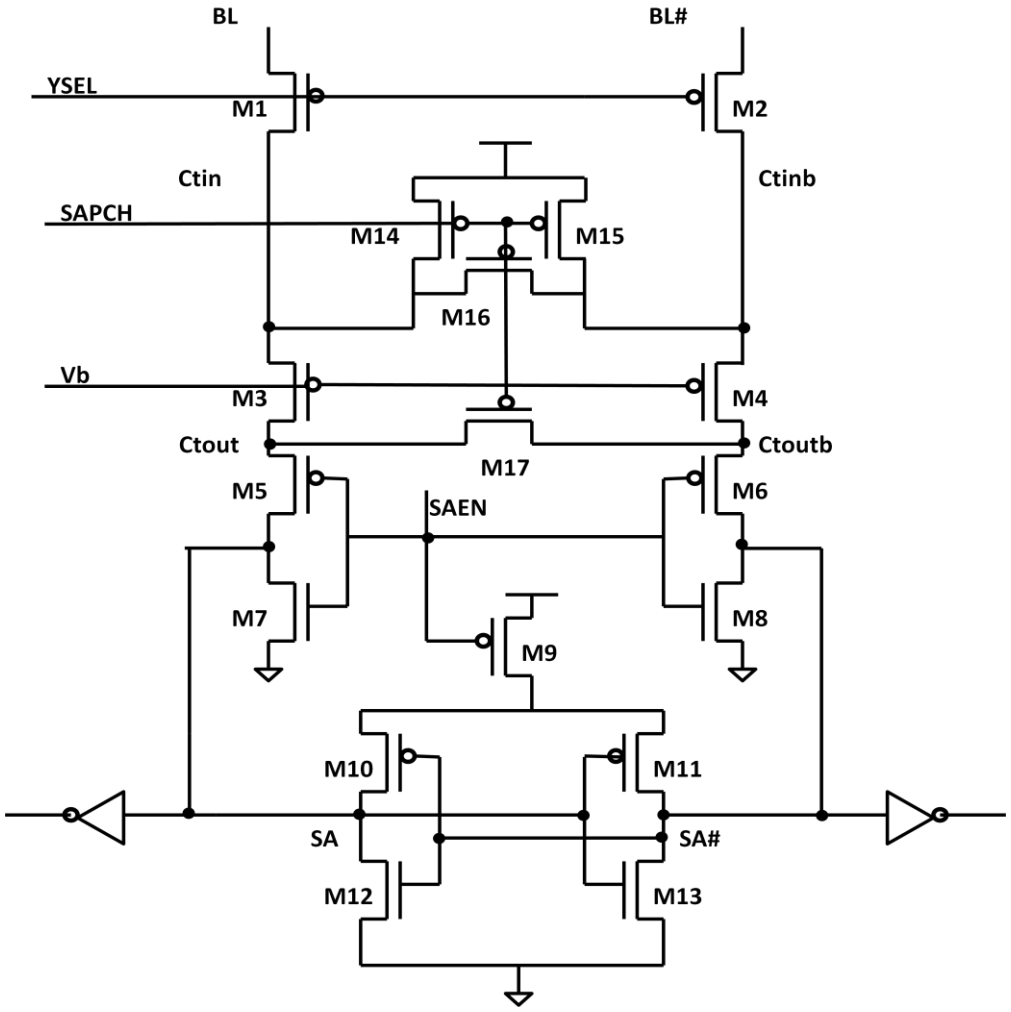


Figure 3.5 Charge Transfer Sense Amplifier

3.3.2 CTSA Operation

The operation of CTSA circuit shown in Figure 3.5 is based on the charge redistribution from high bit-line capacitance to the low capacitance of sense nodes sa and

sa#. This charge redistribution results in high speed operation and low bit-line swing. The circuit consists of two parts. First is the common gate cascode formed by M3, M5 and M7 (and M4, M6 and M8), with PMOS devices M3 and M4 biased at Vb. Second, the cross-coupled inverters formed by M9 through M13, latches the output of the common-gate amplifier (sa and sa#).

In the precharge phase, the bit-lines and all the intermediate nodes (ctin, ctinb, ctout, ctoutb) are precharged high. The output of the common gate amplifier (sa and sa#) are predischarged low by keeping SAen high. In the evaluation phase, SAPCH is pulled high and YSel is grounded to select a column. CTSA is enabled by pulling SAen low. Suppose the bit-line bl# is going low. As the voltage of bl# goes near Vb + Vtp, M4 goes into sub-threshold region of operation preventing the output node sa# from getting charged. However, the other bit-line bl remains high and charges the output node sa to high. Initially NMOS pair M12 and M13 helps in rejecting the common mode noise and thereafter helps in latching the value sensed by the common gate amplifier. The timing scheme of the CTSA is shown in Figure 3.6.

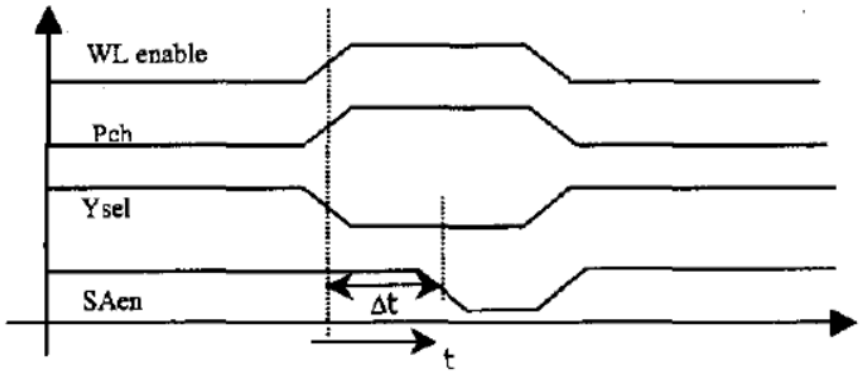


Figure 3.6 Timing Scheme for CTSA [6]

3.4 Current Latched Sense Amplifier

The circuit diagram of a current latched sense amplifier is shown in Figure 3.7.

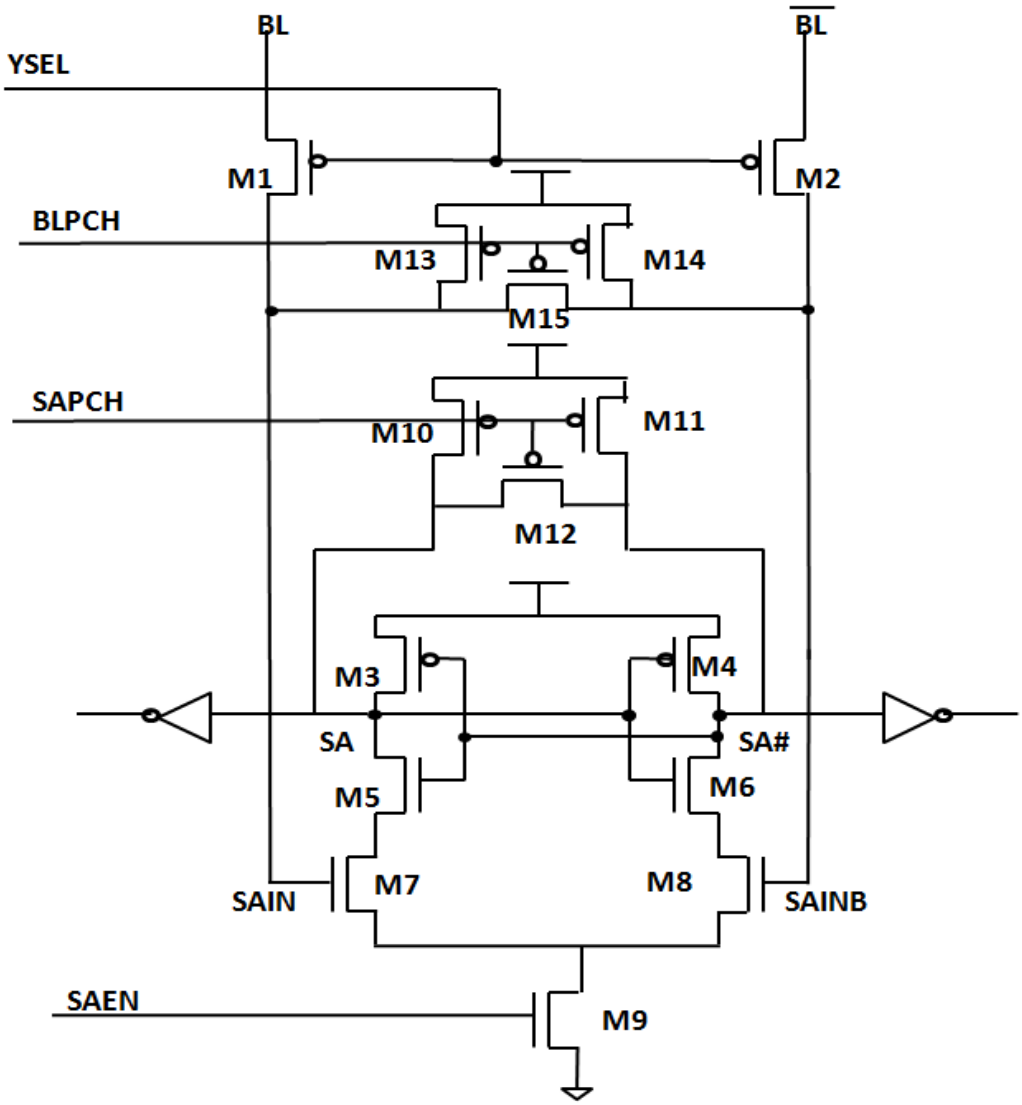


Figure 3.7 Current Latched Sense Amplifier

The operation of the circuit is as follows. The differential voltage on bit-lines is passed onto SAIN and SAINB inputs of the CLSA. When SAEN is pulled high, both

outputs SA and SA# start discharging. Let us say, SAIN = VDD and SAINB = VDD-ΔV. This results in higher current through M7 than M8 due to its higher Vgs. This causes output SA to discharge faster than SA#. When SA has fallen low enough to turn ON PMOS device M4, the strong positive feedback loop is activated, causing SA# to be charged back to VDD and SA to fall to VSS. Unlike the Voltage Sense Amplifier, the CLSA has its outputs isolated from the inputs.

Chapter 4. Design and Simulation

The sense amplifier designs were characterized in an SRAM array with 128 cells connected to the word-line and 128 cells in each column connected to a bit-line. A 4:1 column mux selects one of the four columns whose output is fed to the sense amplifier. A critical path model of the 128x128 array is built as shown below.

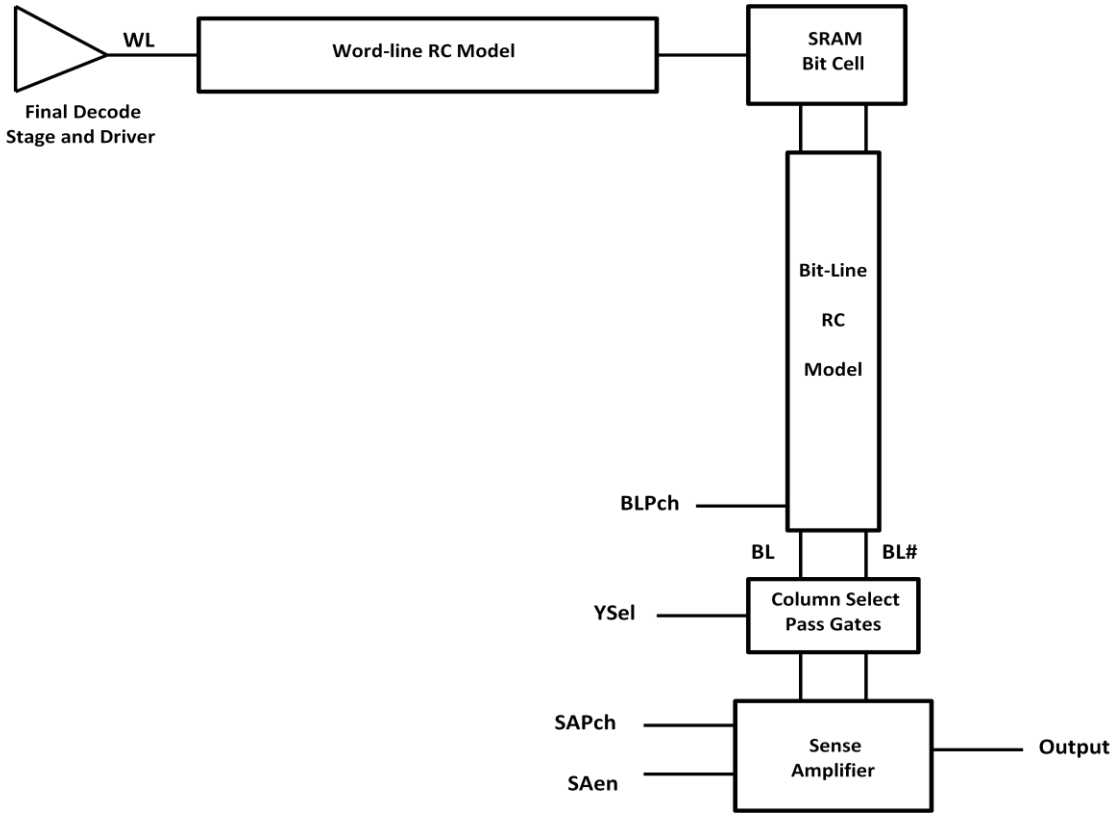


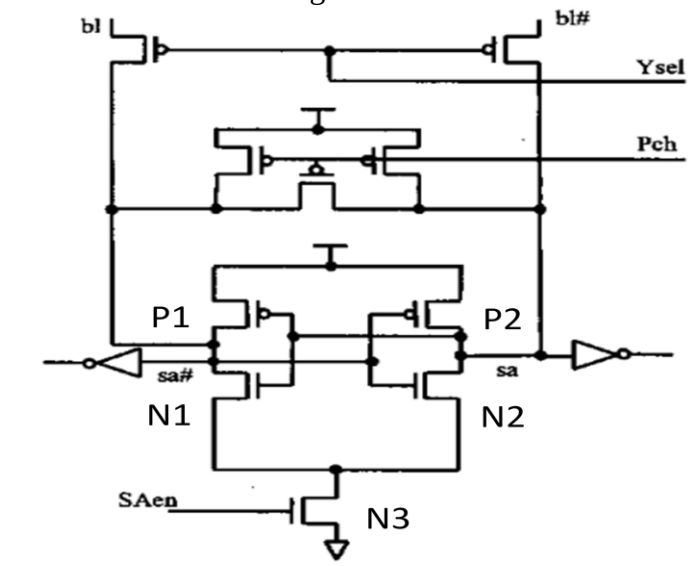
Figure 4.1 Simulation model for a 128x128 SRAM array

The model includes final word-line decoder and driver, as well as the output load for the sense amplifier. Bit-lines and word-line are modeled using π-4 model distributed interconnects. Device loads including those on the bit-lines, word-line and column muxes

are included in the model. The bit-line precharge, sense-node precharge and column mux circuits and their device sizes are kept identical in all cases. The time between word-line enable and sense amplifier enable (SAen) is swept to sense increasing differential voltages or currents. The total read delay is the sum of word-line to sense-amplifier enable delay and the delay of the sense amplifier itself, which is measured from sense amplifier enable assertion to the sense amplifier output inverter switching to 50% of its final value. The energy numbers are measured from the average current normalized to the time period and are therefore frequency independent. The voltage sense amplifier (VSA), a current latched sense amplifier (CLSA), a clamped bit-line current sense amplifier (CSA) and a charge transfer sense amplifier (CTSA) were designed and characterized to understand their speed, power consumption and area relative to each other.

4.1 Voltage Sense Amplifier Design and Simulations

The voltage sense amplifier circuit was tuned and the following transistor sizes were arrived at as shown in figure 4.2



Device	W/L (um)
P1/P2	1/0.05
N1/N2	5/0.05
N3	4.5/0.05

Figure 4.2 Voltage Sense Amplifer Design and Transistor Sizing

The pmos devices P1 and P2 can be sized small since the output nodes sa and sa# are precharged high before the start of sense operation and don't need to be pulled up by P1 and P2. The nmos devices N1 and N2 in the cross coupled inverter pair as well as the enable device N3 need to be sized for speed since they are in the critical discharge path. From a raw performance standpoint, you get a few picoseconds of speed improvement if the N3 device is sized higher and the N1/N2 devices correspondingly sized smaller than the numbers given above. But higher widths on N1 and N2 are very important due to process variations as described in [12]. This effect, though not explored in this report, was considered in the relative sizing of nmos devices N1-N3. Due to process variations like random dopant fluctuations, Vt of transistors have random variations which cause mismatch among neighboring transistors. This can induce trip point mismatch among the cross coupled inverters of voltage sense amplifiers, resulting in operational failures. Under threshold variation, different trip point voltages are developed for the two inverters in the circuit. The initial voltage difference at the output nodes created by bit-line voltage difference may not result in the flipping of the cross-coupled inverters in the right direction if there is sufficient trip point voltage mismatch to offset the difference. Upsizing widths of N1 and N2 is effective in reducing the failure probability because it reduces Vt variation and hence trip point mismatch. Increasing the width of N3 does not lower failure probability because it is a common transistor for the two paths and its variation affects both paths equally.

4.1.2 Characterization Results and Waveforms.

The simulation waveforms of the voltage sense amplifier are shown in Figure 4.3

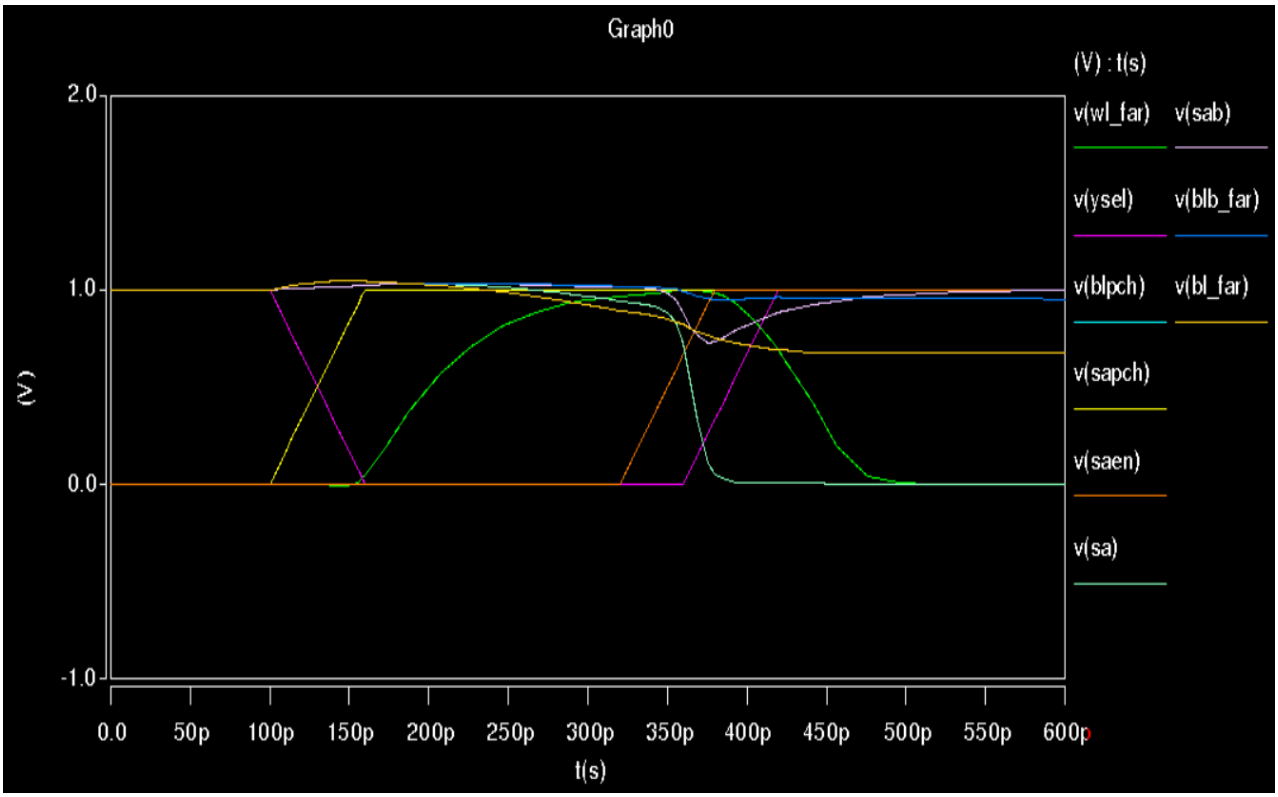


Figure 4.3 Voltage Sense Amplifier Waveforms

Bit-line precharge and sense node precharge signals are turned off and YSel is pulled low to turn on the column mux. When WL is enabled, differential begins to develop on the bit-lines which is then transferred to the sense amplifier nodes sa and sa# through the column select pass gate. When enough differential has developed on the sense nodes, SAen is pulled high and one of the sense amplifier outputs (sa in this case) is pulled low, while the other output (sa# here) remains high. About two gates after SAen assertion, YSel is pulled high to turn off the column mux pass gate. This helps prevent the bit-lines from being quickly discharged by the sense amplifier output which discharges full rail to

VSS. Around the time the column mux is shut off, WL is also disabled to prevent the bit cell from further discharging the bit-lines thereby reducing dynamic power. The waveform shows the bit-line clamped at a higher voltage rather than going all the way to VSS. The current waveform during read with a voltage sense amplifier is shown in Figure 4.4.

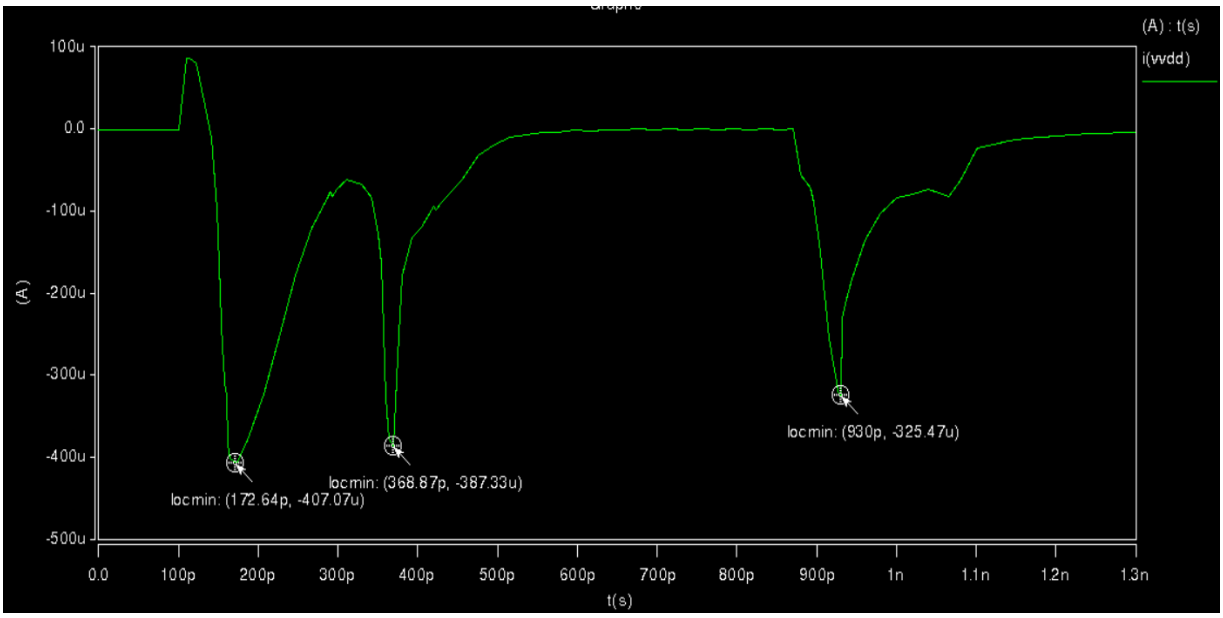


Figure 4.4 Current Waveform of a Voltage Sense Amplifier

The major components of power during a read operation with a voltage sense amplifier are shown above. The first current peak at 172ps corresponds to the switching of word-line, YSel and precharge signals. The second peak at 368ps corresponds to sense amplifier enable and associated sense node discharge. The third peak at 930ps is at the end of the read operation when the bit-lines and sense nodes are precharged to full VCC to prepare for the next access. Figure 4.5 shows how the VSA delay varies as word-line to sense amplifier enable delay is increased. The differential voltage on the sense

amplifier nodes increases with increasing WL to SAen delay and therefore results in decreasing sense amplifier delay.

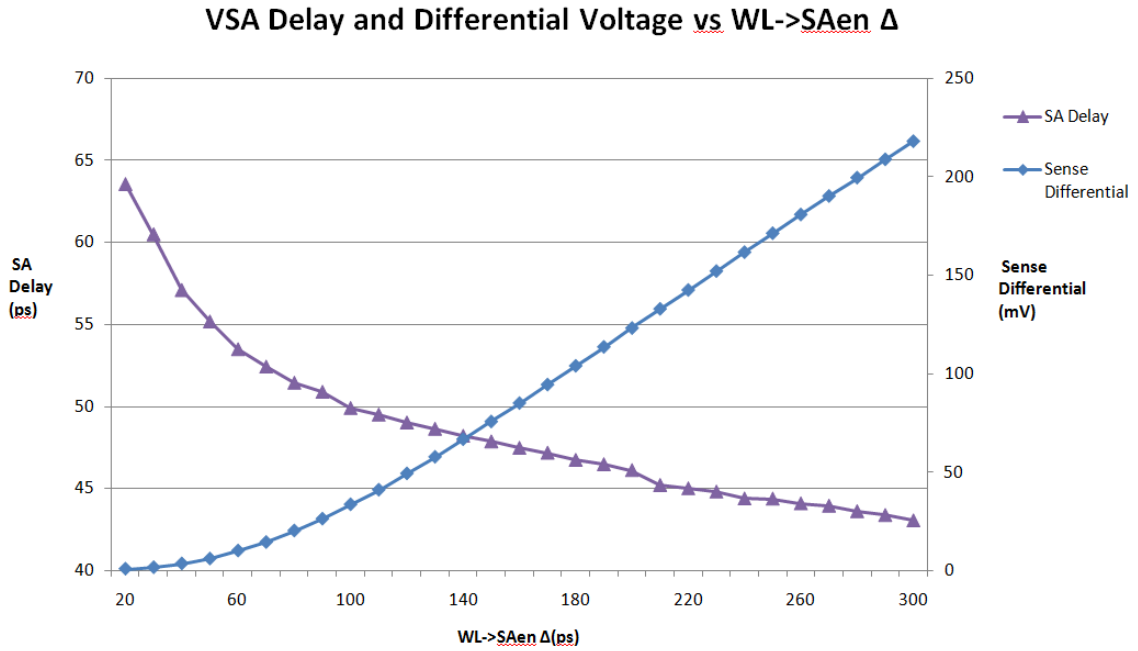


Figure 4.5 Delay and Differential Voltages for VSA

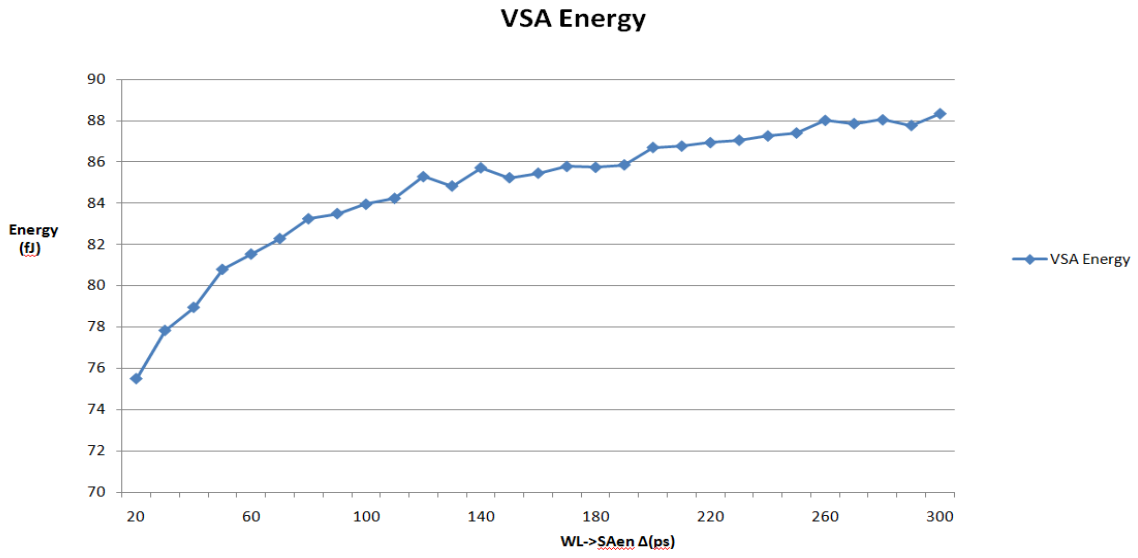
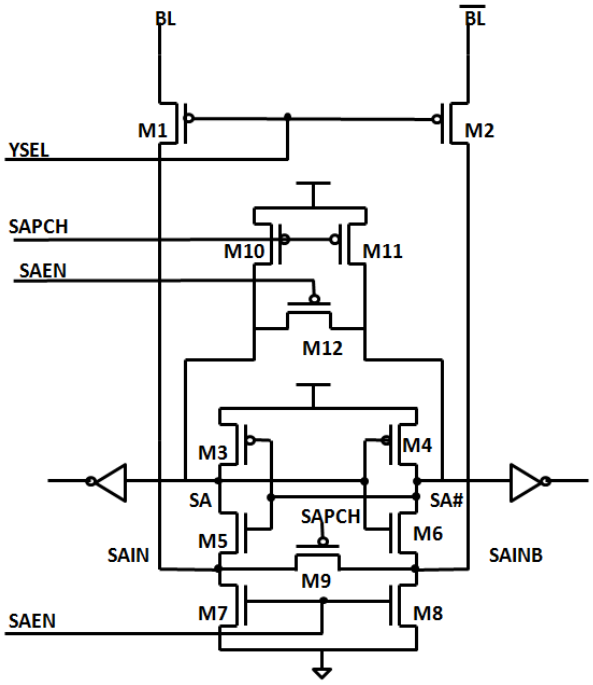


Figure 4.6 Energy for VSA

Figure 4.6 shows how the total energy associated with the read operation changes with increasing WL to SAen delay. As described by the current waveform in Figure 4.4, the total power is composed of the dynamic power due to switching of word-line and other control signals, the read power as the bit-lines and sense nodes discharge through the bit cell, the sense amplifier enabling power and finally the precharge power to bring bit-lines and sense nodes to VCC. As WL to SAen delay increases, the low going bit-line falls to lower voltage levels resulting in higher precharge power at the end of the read operation.

4.2 Current Sense Amplifier Design and Simulations

The current sense amplifier circuit was designed with the following transistor sizes as shown in Figure 4.7



Device	W/L (um)
M3/M4	1/0.05
M5/M6	1/0.05
M7/M8	1/0.05
M9	2/0.05

Figure 4.7 Current Sense Amplifier Design and Transistor Sizing

The voltage waveforms for a current sense amplifier are similar to that of a voltage sense amplifier as shown in Figure 4.8.

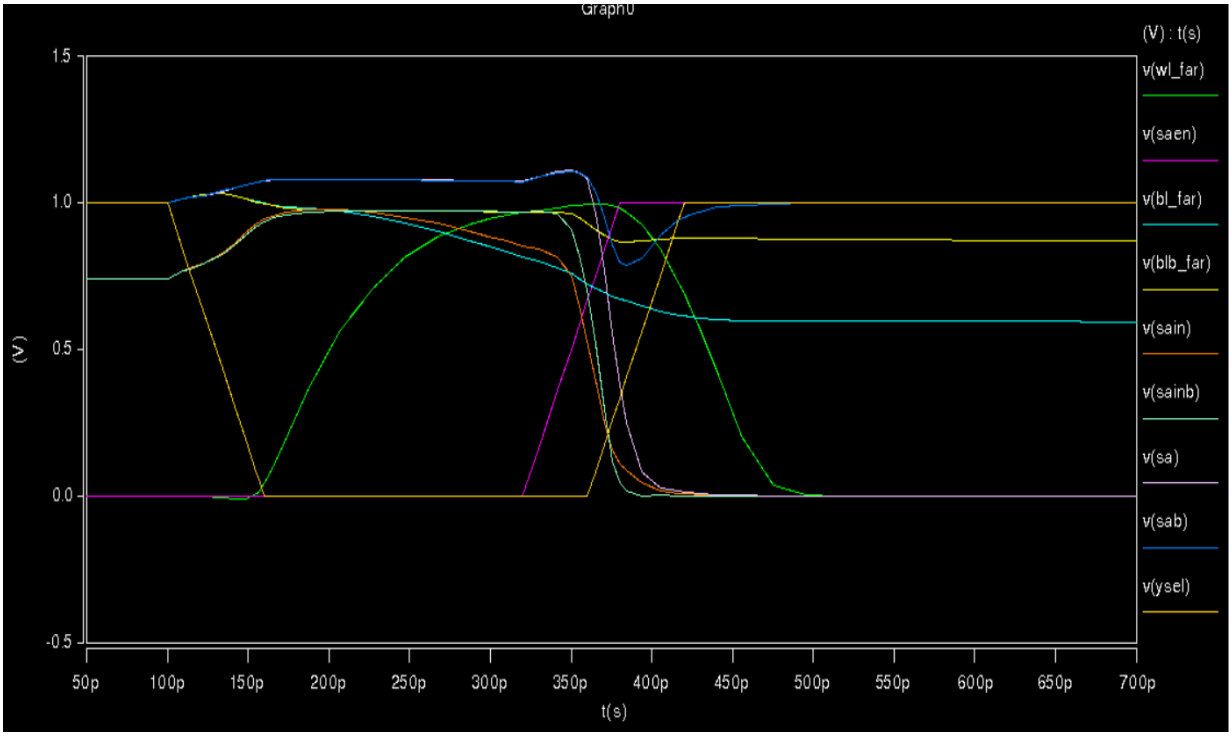


Figure 4.8 Current Sense Amplifier Waveforms

However, the CSA operates by sensing the current difference on the bit-lines. When SAen is enabled, the differential current on the legs of the sense amplifier gets converted to a differential voltage on the output nodes which are then quickly amplified to full swing output by the positive feedback of the cross coupled inverters. The current waveforms through the two legs of the CSA when SAen is asserted is shown in Figure 4.9.

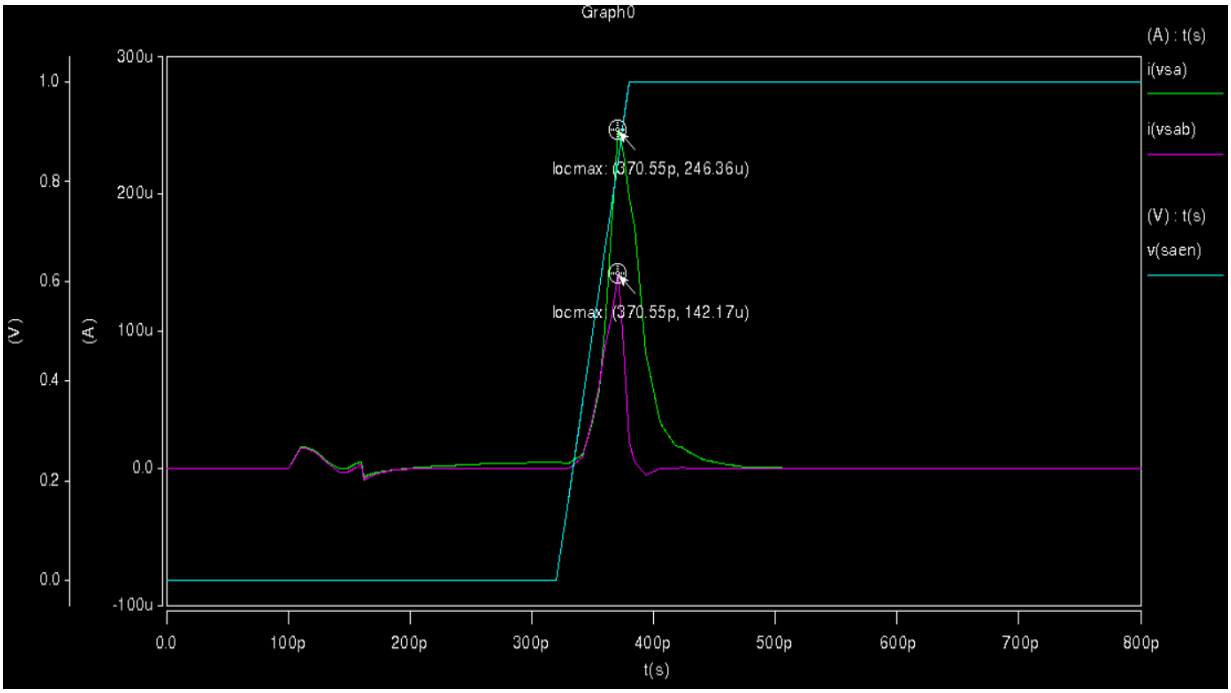


Figure 4.9 CSA current waveforms

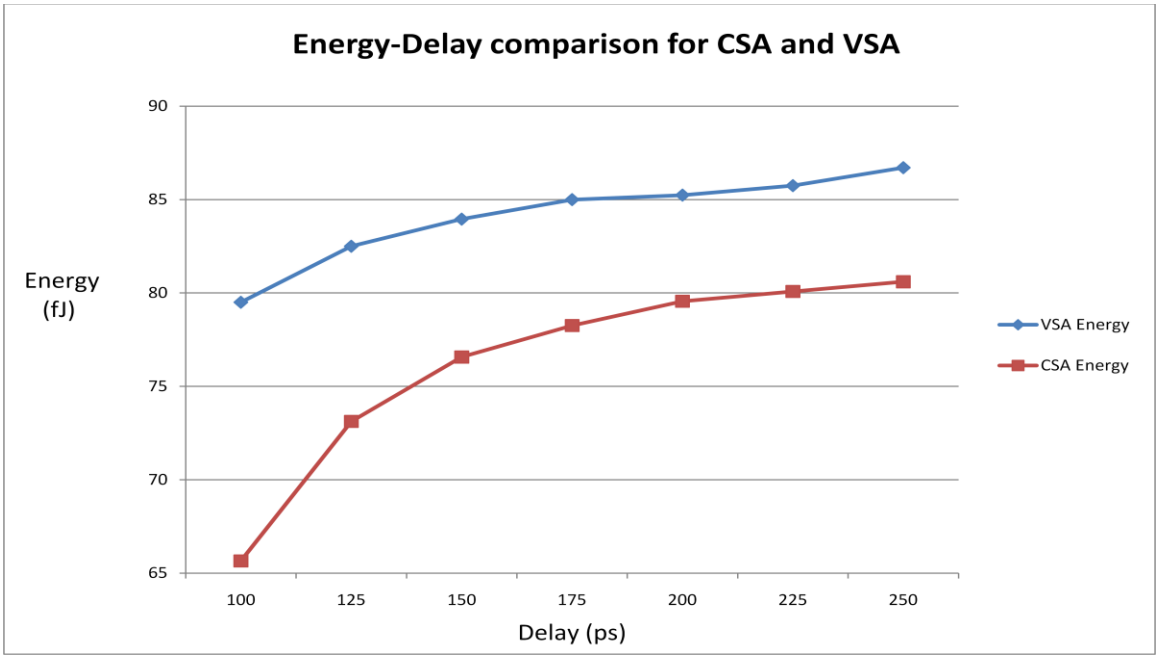
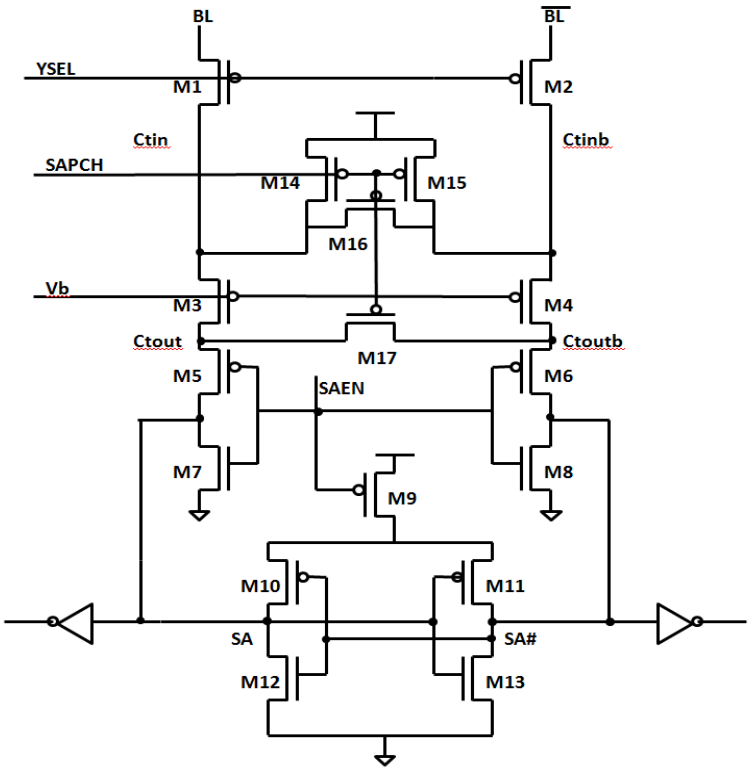


Figure 4.10 Energy Delay Comparison between Voltage and Current Sense Amplifiers

Figure 4.10 shows the energy-delay curves for voltage and current sense amplifiers. It shows that for the same total read access delay, CSA has 7-17% lower energy than the VSA. For a given WL to SAen delay, VSA is on the average 15ps faster than the CSA. But the CSA can be designed for much smaller area with negligible loss in performance. The CSA circuit here has half the area compared to the VSA. Therefore, the CSA occupies much smaller area and consumes half the energy for a given delay compared to the VSA. This makes the CSA a better choice for low power designs and area constrained designs compared to the VSA, with a minimal loss in performance. The current conveyor circuit shown in the previous chapter doesn't work well at low voltages and was therefore not used in the CSA design shown here. It also shows sensitivity to the Vt of devices, not making it a good choice in the face of process variations.

4.3 Charge Transfer Sense Amplifier Design and Simulations

The charge transfer sense amplifier circuit was designed with the transistor sizes as shown in Figure 4.11. The bias voltage Vb is set at 0.4V. It is critical to set this voltage at the right value as the charge transfer device M3/M4 cuts off when its input source voltage falls to Vb+Vtp. Setting Vb at a higher value causes the charge transfer device to be cut off early and not have the differential voltage propagate to the sense nodes sa and sa#. Setting this voltage too low prevents the charge transfer device from entering the sub-threshold region and causes the cross coupled positive feedback inverter to further discharge the bit-line resulting in higher precharge power.



Device	W/L (um)
M3/M4	2/0.05
M5/M6	1/0.05
M7/M8	0.25/0.05
M9	6/0.05
M10/M11	1.5/0.05
M12/M13	0.5/0.05
M17	0.5/0.05

Figure 4.11 Design and Transistor Sizing of Charge Transfer Sense Amplifier

The read waveforms for a charge transfer sense amplifier are shown in Figure 4.12. The differential voltage on the bit-lines propagate to the inputs of the charge transfer devices M3 and M4 (ctin and ctinb) through the column select mux and further to their output nodes (ctout and ctoutb). When enough differential has developed on the nodes ctout and ctoutb, the sense amplifier is enabled by pulling the sense enable low. The positive feedback loop takes over and quickly amplifies the differential voltage to full swing output. The low going ctout node is pulled low by the sense node while the charge transfer device M3/M4 cuts off when ctin falls to Vb+Vtp. This results in significant savings in bit-line precharge power. The current waveform is shown in Figure 4.13.

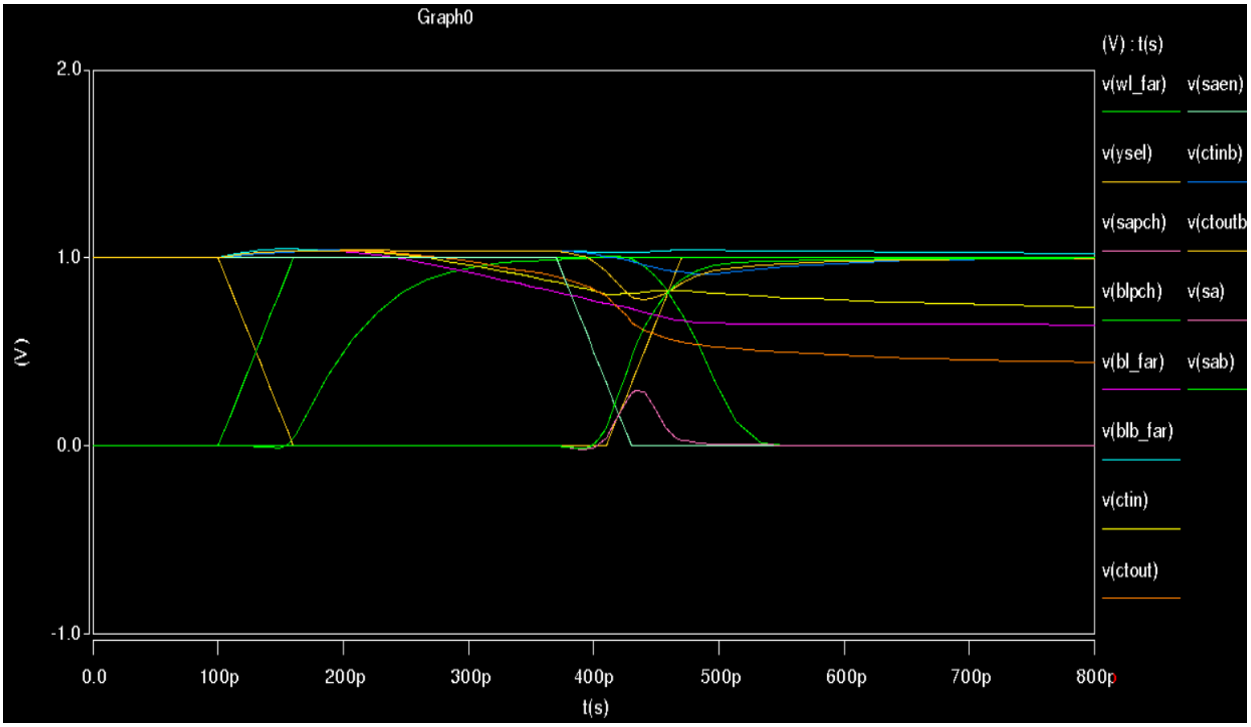


Figure 4.12 Read waveforms for a Charge Transfer Sense Amplifier

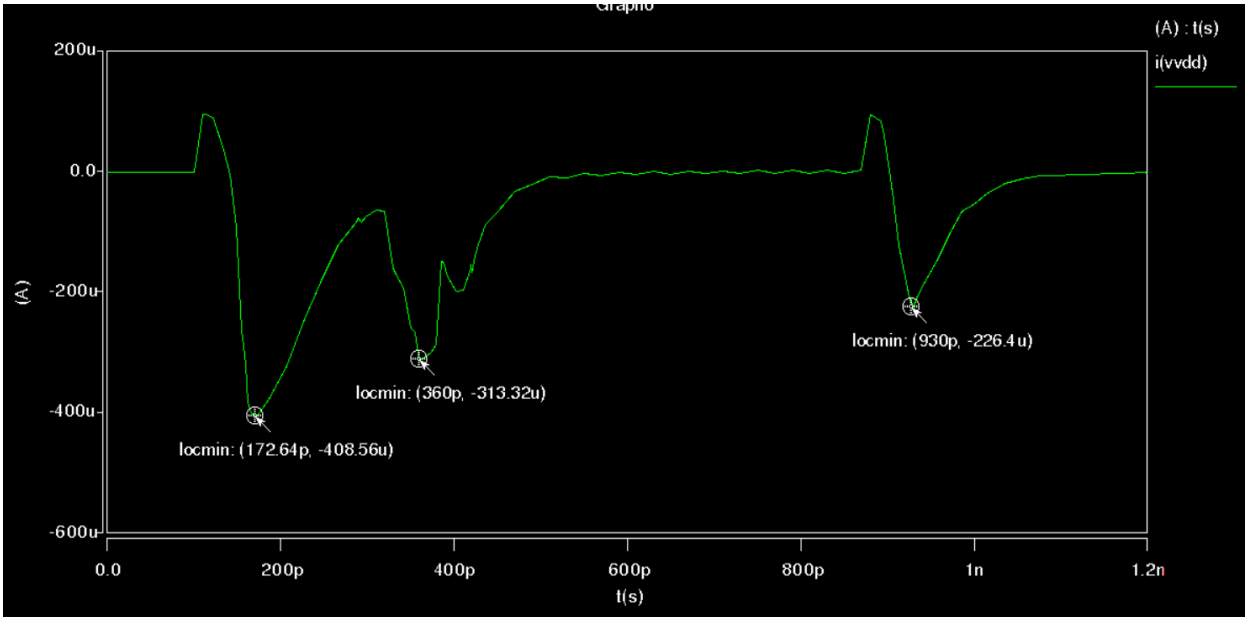


Figure 4.13 Current Waveform during read with a CTSA

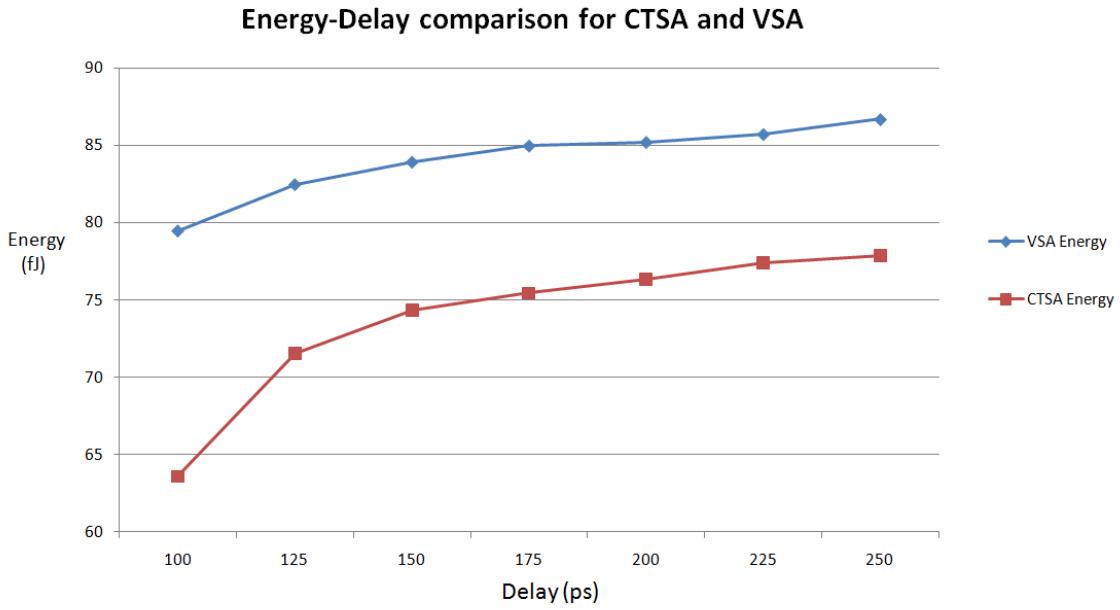
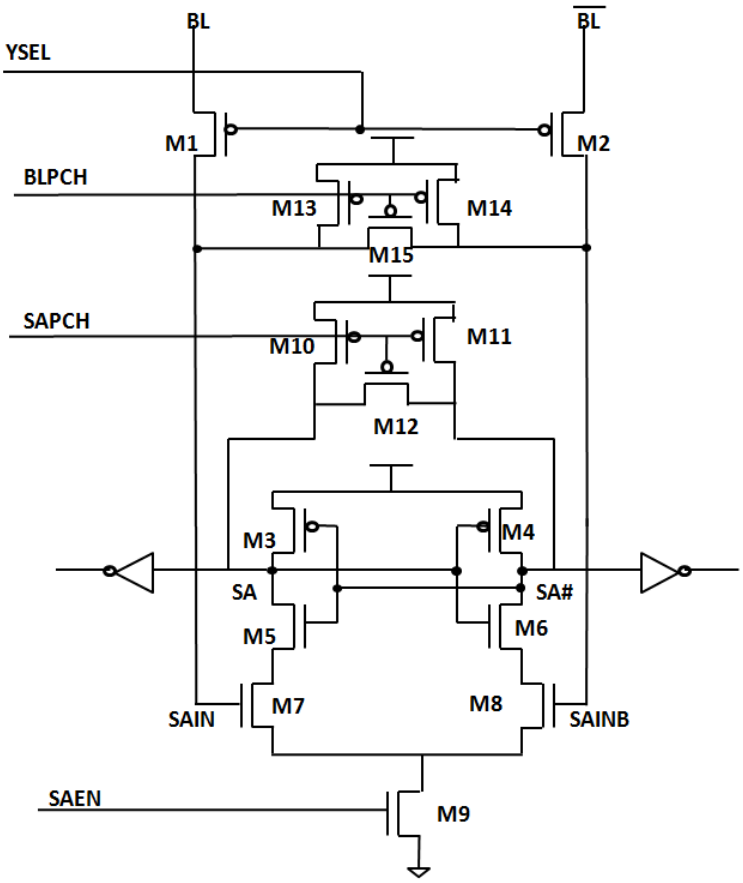


Figure 4.14 Energy Delay Comparison between VSA and CTSA

The energy delay comparison between a CTSA and VSA is shown in Figure 4.14. For a given delay, the CTSA burns lower power than both VSA and CSA. The CTSA design here has the same area as the VSA. The CTSA has 10-20% lower energy compared to VSA for the same delay. The difference comes mostly from the precharge power since the bit-line is cut off from the sense node by the charge transfer device. The CTSA has on the average about 12ps more delay than a VSA.

4.4 Current Latched Sense Amplifier Design and Simulations

The current latched sense amplifier (CLSA) was designed with the device sizes as shown in Figure 4.15.



Device	W/L (um)
M3/M4	1/0.05
M5/M6	2.5/0.05
M7/M8	2.5/0.05
M9	4.5/0.05
M13/M14/M15	0.2/0.05

Figure 4.15 Current Latched Sense Amplifier Design and Transistor Sizing

The total device width was kept the same as voltage sense amplifier and the energy-delay numbers were compared. The energy-delay comparison between current latched and voltage sense amplifiers is shown in Figure 4.16.

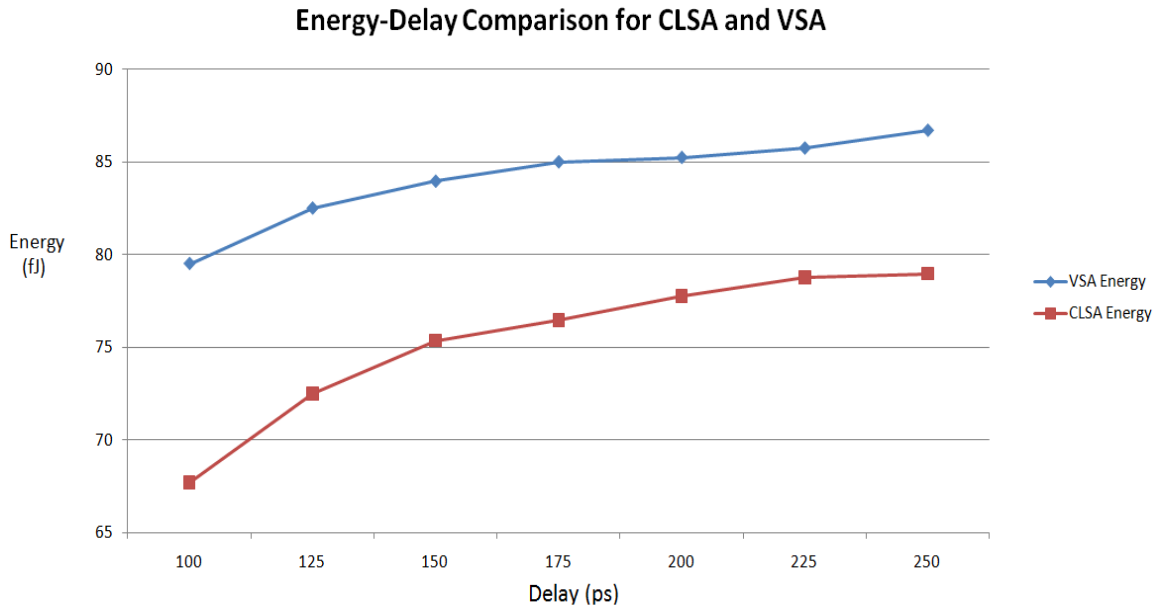


Figure 4.16 Energy Delay Comparison between VSA and CLSA

The comparison curves show that CLSA has 8-15% less energy than VSA for a given delay. The lower energy can be attributed to lower operating current when SAEN is enabled due to the larger number of transistors in the stack. The CLSA also has lower energy numbers than a CSA, but has twice the total device width and therefore twice the area of a CSA. Of the four sense amplifier circuits, CTSA has the lowest energy numbers for a given delay. But CTSA has additional complexity due to the requirement of a bias voltage generator for the charge transfer device.

Chapter 5. Conclusion

This report presented the design and analysis of four different sense amplifier topologies – Voltage Sense Amplifier (VSA), Current Latched Sense Amplifier (CLSA), Clamped Bit-line Current Sense Amplifier (CSA) and Charge Transfer Sense Amplifier (CTSA). The sense amplifiers were characterized to find out their relative performance, energy and area. The sense amplifiers were analyzed in a 128x128 SRAM array for which a 6-T SRAM bit cell was designed. All work was done on 45nm bulk CMOS technology.

The Voltage Sense Amplifier is the most commonly used in SRAM designs and is the simplest of them all. It showed the highest performance in simulations. The Current Sense Amplifier (CSA) operates by sensing the cell current directly rather than waiting on a voltage differential on the bit-lines. Although some papers [5] show 15-20% better speed on the CSA delay, it was hard to beat the performance of a VSA on a 45nm process. Besides, the total read access time is given as the sum of WL to SAen delay and the sense amplifer delay itself. In this context, 10-15ps improvement in the delay of the sense amplifier itself is pretty insignificant. The earliest point at which the sense amplifier can be enabled is determined by statistical simulations for very deep sub-micron processes, which is not in the scope of this report. But this work shows that for the same total read access delay, CSA has 7-17% lower energy than the VSA. The CSA has half the area compared to the VSA which is pretty significant.

The charge transfer sense amplifier (CTSA) operates by making using of the charge transfer mechanism between the high capacitance bit-lines and low capacitance sense amplifier output nodes. Characterization results show that for about 12ps higher delay

compared to the VSA, the CTSA consumes 10-20% lower energy for the same area. CTSA has the lowest energy of all the sense amplifiers analyzed here. CTSA needs an additional bias voltage generator for the charge transfer device, this can be placed in the control section and shared between all the sense amplifiers in the memory.

The current latched sense amplifier (CLSA) consumes 8-15% less energy for a given delay and area compared to the voltage sense amplifier. The CLSA also has smaller energy numbers than the CSA, but has twice the area of a CSA.

Future work would include statistical Monte Carlo simulations to find out the impact of process variations on the performance of these sense amplifiers. This will tell us the earliest point at which they can be enabled relative to word-line assertion and therefore give a better picture of their relative speeds.

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Vita

Sajith Ahamed Palatham-Veedu graduated with a Bachelor's degree in Technology from Cochin University of Science and Technology, India in 1997. Since then he has been working in the semiconductor industry for companies including Alliance Semiconductor, Silicon Graphics Inc, Advanced Micro Devices Inc and is presently with Intel Corporation, Austin. Sajith has worked on circuit design and implementation for high performance and low power microprocessors, network processors and SOCs. In his spare time, he likes spending time with his wife and kid, travelling, hiking, reading and watching movies.

Permanent address : 7905 Alophia Dr, Austin, TX 78739

This report was typed by the author.